Annexure – I

NIELIT CHENNAI

Program Details

"Digital System Design using Verilog HDL**"**

Objective **:** To provide exposure in Designing Digital Systems using Verilog HDL Language.

Target Audience : Students of Engineering Institutions

Batch Size **: Max 30 Nos**

Topics covered : 1.Getting Started with Icarus & Sigasi Tools and Overview of Verilog HDL.
2. Hierarchical Modeling concepts.
3. Datatypes,Modules & Ports.
4. Types of Modeling.
5. Task & Functions.
6. Logic Synthesis.
7. Combinational & Sequential Circuits.
8. Synchronous & Asynchronous Sequential Circuits.
9. Introduction to FPGA.
10. Synthesis,Simulate and Generation of Bit stream.
11. Implementation in Spartan 6.

Duration : Starting Date: 11-09-2017 Ending Date: 25-10-2017
(Training 100 hrs + Mini Project 20 hrs)

Timing : 01:30 PM to 05:30 PM

Venue **:** NIELIT CHENNAI

Course fee : Rs.4,000/- (Inclusive of Service Tax)

Course in-charge **: KARTHICK RAJAN, Project Associate**
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