National Institute of Electronics and Information Technology, Chennai

COURSE PROSPECTUS

Name of the Group:	VLSI- ES & AE
Name of the Course:	Certificate Course in **VLSI Design**
Course Code:	VL100
Starting Date:	16th December 2019
Duration:	80 Hrs
Course Coordinator:	Karthick Rajan. N
Course In charge:	Ishant Kumar Bajpai, M: +91-9958016673, Email: ishant@nielit.gov.in
Last date of Registration:	12th December 2019

Preamble:

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general purpose processors and ASICs. In particular, high performance systems are now almost always implemented with FPGAs.

As per the recently published data, there are over 20,000 engineering professionals are working in more than 150 companies in chip designing industry and there is a huge demand for high quality trained manpower in this field.

This program will enhance the career opportunities of the participants by up skilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Objective of the Course:

Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. In this process participant will acquire expertise on entire logic design process and will be able to take on the challenges posed by chip design industry.

Outcome of the Course:

After successful completion of this Course, the participants shall able to:

1. Design Control and Data path Units
2. Author Design IPs for VLSI using Verilog HDL
3. Develop Test Benches using Verilog HDL
4. FPGA based prototyping using Verilog HDL

Course Structure:

S.No	Topics	Duration(in Hrs.)
1	Advanced Digital Design Review	12
2	Hardware Description Language (Verilog HDL)	40
3	FPGA Architecture and Prototyping	28
	Total	**80**

Other Details:

Course Fees:

For General Candidates: Course fee is **Rs. 4,500/-(Including GST)**

For SC/ST Candidates: No Fee

However they are required to remit an amount of **Rs.1,000/-**as advance security deposit. This amount will be considered as security deposit and will be refunded after completion of the course. If the student fails to complete the course successfully this amount along with any other security deposits will be forfeited.

Registration Fee:(Non-refundable)

SC/ST: No registration fee

Others: **Rs.500/-(Including GST)**

However the above registration fee shall be refunded on few special cases as given below:

1. If course postponed and new date is not convenient for the student.
2. If course cancelled.

Payment schedule: The Fee is to paid in one instalment as given below.

Instalment No.	Last Date for Payment	Amount (in Rs.)
1.	12-12-2019	5,000/-

Eligibility: Pursuing Engineering Degree [ECE/EEE/CSE/AEI]

Number of Seats: 30

How to apply:

National Institute of Electronics and Information Technology, Chennai

Candidates are advised to download the Registration from our website www.nielit.gov.in/chennai. After filling the form with all documents and fees, it can be submitted to NIELIT Chennai office in person or through post before staring of the course. Payment towards non-refundable Registration and Course fee canbe paid through any one of the following modes:

- ✓ DD drawn from a nationalized bank (preferably SBI) in favour of "NIELIT Chennai" payable at Chennai.
- ✓ Online transaction: Account No: 31185720641 Branch: Kottur (Chennai), IFS Code: SBIN0001669.
- ✓ Pay through Nationalized Bank Debit Card (Service charges applicable)

  Note: The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

Last date of Registration: 16th December 2019

Selection of candidates: First Come First Serve basis

Admission Procedure:

All interested candidates are required to fill the Registration form with the fees (Registration and Course fees) before 16th December 2019 with all the necessary following documents.

- Original and self-attested Copies of Proof of Age, Qualifications, etc.
- One passport size photograph and one stamp size photograph for identity card.
- Self-attested copy of Govt. issued photo ID card (AADHAR is mandatory for SC/ST Candidates).
- Self-attested copy of community certificate (if availing SC/ST fee concession)

Note: Working days are from Monday to Friday. Admission timings are from 9.00 am to 5.30 pm.

Discontinuing the course: No fees under any circumstances shall be refunded in case of a student discontinuing the course. No certificate shall be issued if discontinued.

Course Timings: Full-time: 9:30 AM to 5: 30 PM (Monday to Friday)

Location: NIELIT Chennai is located at Gandhi Mandapam Raod, Kotturpuram, Chennai (Landmark: Opp. To Anna Centenary Library)

Address: National Institute of Electronics and Information Technology Chennai Centre,
ISTE Complex, No. 25, Gandhi Mandapam Road,Chennai – 600025
E-mail: training.chennai@nielit.gov.in / Phone: 044-24421445
Contact Person: Karthick Rajan. N, Mobile: 9080298798, 9940569468

Course enquiries: Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

Lab Facilities: Xlinx Design tool, Atlys Spartan-6 FPGA Development Kit, DE0 Nano & DE2-115 Development Board, Xilinx Kintex-7 FPGA KC705 Evaluation Kit, Xilinx Zyng-7000 SoC Video and imaging kit, ZedBoard Zyng-7000 Development Board, and Logic Analyzer

Annexure

Detailed Syllabus of the Course

1. **Advanced Digital Design Review:**
   Duration: 12 Hours

   Objective The objective of the course is to provide understanding of the entire logic design process with the analysis from combinational and sequential digital circuit design. Course Description

   - ✓ Combinational Circuit Design
   - ✓ Sequential Circuit Design
   - ✓ Design of controller and Data path units
   - ✓ State Machines
   - ✓ Controller Design using FSMs & ASMs
   - ✓ Design Examples & Case Studies

Text Books: 1. Modern Digital Electronics by R P Jain, Edition 3, Tata McGraw-Hill Education
2. Digital Design Principles and Practices by Wakerly, John F,

2. **Hardware Description Language (Verilog HDL)**
   Duration: 40 Hours

   Objective The objective of the course is to provide understanding of the techniques essential to the Verilog programming for Verification and Testing.

   - ✓ Introduction to Verilog HDL & Hierarchical Modelling Concepts
   - ✓ Lexical Conventions & Data Types
   - ✓ System Tasks & Compiler Directives
   - ✓ Modules, Ports and Module Instantiation Methods
   - ✓ Modelling methods.
   - ✓ Design Verification using Test benches

Reading List: Verilog HDL, 2/E By Samir Palnitkar,Pearson Education

3. **FPGA Architecture and Prototyping**
   Duration: 28 Hours

Objective FPGAs are the present day tool for implementing many embedded applications. A basic understanding of digital electronics is very useful for the proper understanding of this topic. Basics of communication are also covered for further applications. Hands own experiments and a mini-project are included in the module.

- ✓ Introduction to Programmable Logic and FPGAs
- ✓ Popular CPLD & FPGA Families
- ✓ Architecture of popular Xilinx and Altera FPGAs

- ✓ FPGA Design Flow
- ✓ Implementation Details
- ✓ Advanced FPGA Design tips
- ✓ Logic Synthesis for FPGA
- ✓ Static Timing Analysis
- ✓ Design problems (Mini Project)

Reading List: FPGA Users Guides and Datasheets from Xilinx & Altera