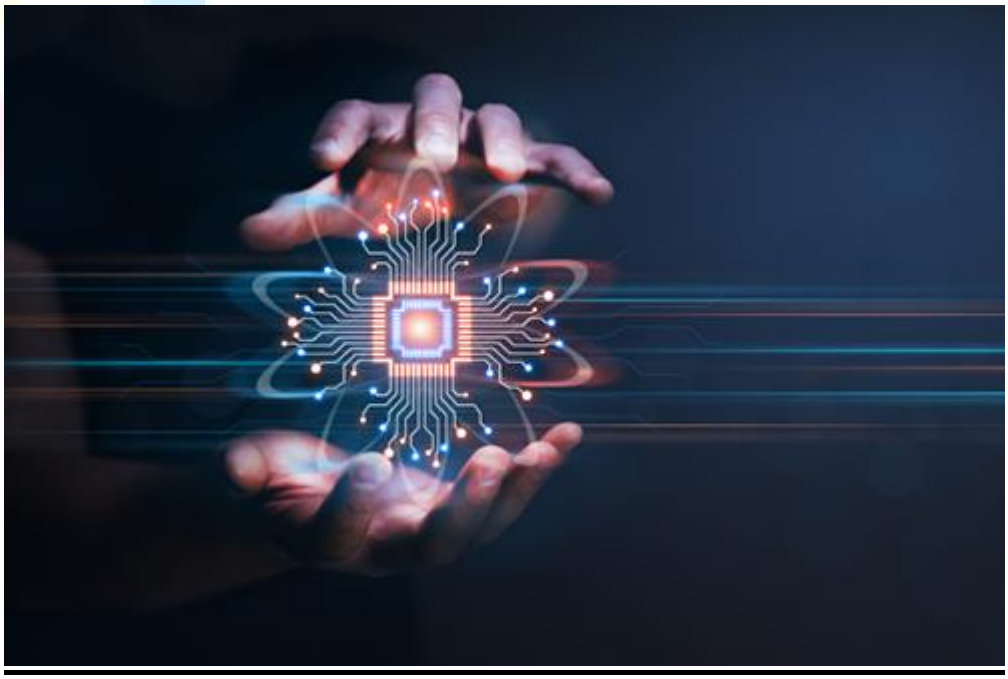
नेशनल इंस्टीट्यूट ऑफ इलेक्ट्रॉनिक्स एंड इंफॉर्मेशन टेक्नोलॉजी, चेन्नई
National Institute of Electronics and Information Technology, Chennai
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

Course Prospectus

Foundation course in VLSI Design

Mode: Online



For Registration visit: https://reg.nielitchennai.edu.in/
Website: https://nielit.gov.in/chennai/index.php

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Course Prospectus

Course Name: Foundation course in VLSI Design (Online Mode)

Course Code: VL31

Duration: 90 hours

Last Date of Registration: 18-02-2024

Date of publishing Provisional Selection List: 20-02-2024

Course Start Date: 22-02-2024

Fee Details:

Registration cum Course Fee- Rs. 6300/-

Preamble:

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general-purpose processors and ASICs. In particular, high-performance systems are now almost always implemented with FPGAs.

As per the recently published data, there are over 20,000 engineering professionals working in more than 150 companies in the chip designing industry and there is a huge demand for high-quality trained manpower in this field. This program will enhance the career opportunities of the participants in upskilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Objective of the Course:

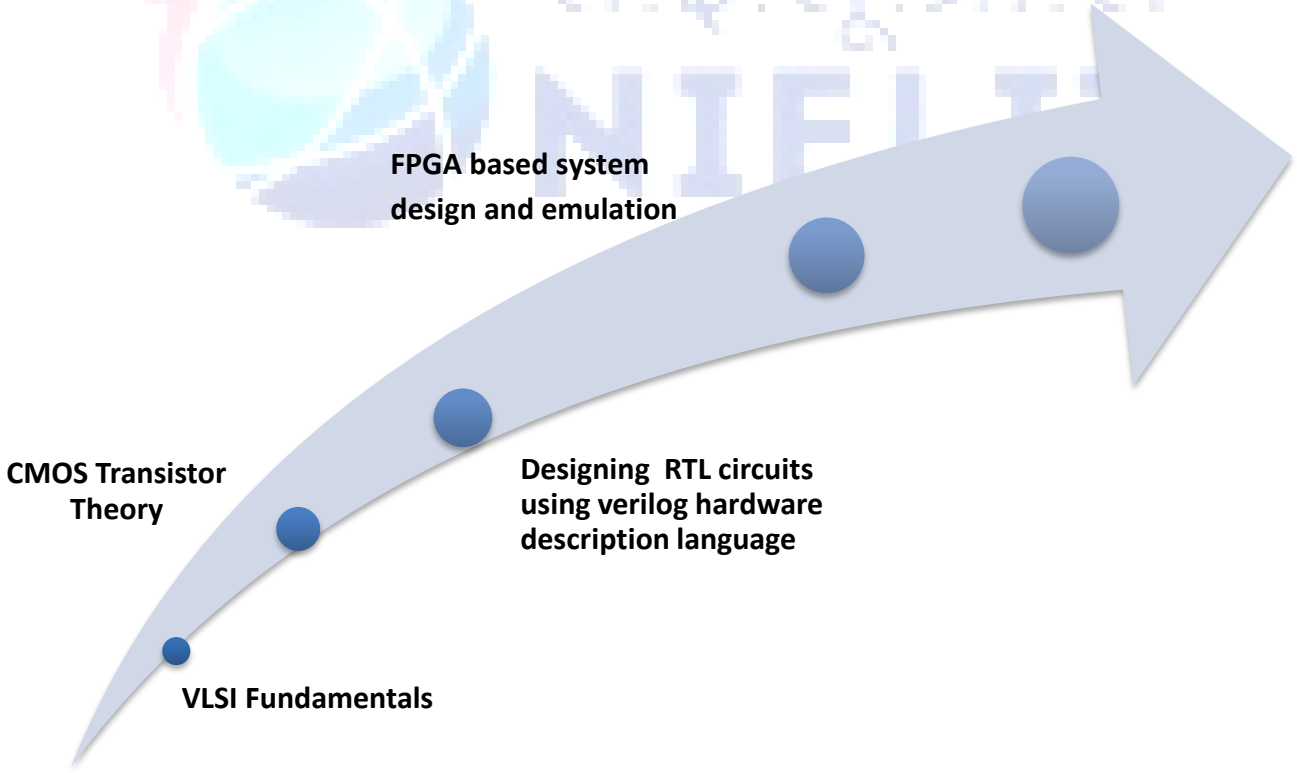
Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. In this process, participants will acquire expertise on entire logic design process and will be able to take on the challenges posed by chip design industry.

Outcome of the Course:

After successful completion of this Course, students will be able to:

- Understand brief history, present and future and Design Cycle of VLSI technology. Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax. Level of Abstraction in Verilog programing writing and simulating test benches in Verilog.
- Design and Develop IPs for VLSI using Verilog HDL and prototype them on FPGAs
- Emulate, debug & Characterize reusable IPs

Full Flow of Course



Course Structure

This course contains a total of 6 module Candidate need to qualify the each module to qualify the Foundation course in VLSI Design program.

Module Code	Module Name	Duration(in Hours)
VL 311	VLSI Fundamentals	15
VL 312	CMOS Transistor Theory	15
VL 313	Designing RTL circuits using Verilog hardware description language	30
VL 314	FPGA based system design and emulation	30
	Total Duration	**90**

Registration cum Course Fees

The course fee is Rs. 6300/- Including GST. (

Registration Fee	SC-ST Candidates (Fee including GST in Rs.)	General Candidates (Fee including GST in Rs.)	Last Date
	1000	6300	18-02-2024

**GST is Applicable as per Govt. Norms GST (currently it is 18%).*

(**Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible.)**

However, the above registration fee shall be refunded on few special cases as given below

- ✓ Candidates are eligible but not selected for admission.
- ✓ Course postponed and new date is not convenient for the student.
- ✓ Course cancelled.

Eligibility

Final Year Polytechnic Diploma in Electronics/Electrical/ Instrumentation or above

Or

3rd semester B.E/B.Tech in Electronics/Electronics & Communication/ Electrical/ Electrical & Electronics/Instrumentation or above

Number of Seats: 30 – Total

Note: Seats are allocated based on the merit of the Qualification.

How to Apply?

Candidates can apply online in our website http://reg.nielitchennai.edu.in. Payment towards non-refundable registration fee can be paid through any of the following modes:

- ✓ Online transaction: Account Name: NIELIT CHENNAI, Account No: 31185720641, Bank name: State Bank of India (SBI), Branch: Kottur (Chennai), IFSC Code: SBIN0001669.
- ✓ Pay through UPI Mobile Apps

Note: *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

Last date of Registration: **18-02-2024**

Registration Procedure

All interested candidates are required to fill the Registration form online with registration fees before **18th February, 2024** with all the necessary information.

Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The first list of Provisionally Selected Candidates will be published on NIELIT Chennai website (www.nielit.gov.in/chennai) **20th February, 2024** by **5:00 PM**. In case of vacancy, an additional selection list will be prepared and the selection will be intimated by email only.

- ✓ Following documents of candidates will be verified(from the registration portal):
  - Self-attested Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheets.
  - One passport-size photograph(to be uploaded to the registration portal).
  - Self-attested copy of Govt. issued photo ID card
  - AADHAR Copy

- ✓ Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

Admission:

All provisionally selected candidates whose documents are verified and paid the fees and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credential and URL for online portal will be shared through WhatsApp or email.

Discontinuing the course

- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

Address:

National institute of Electronics and Information Technology
ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025
Telephone:044-24421445

Course enquiries

Students can enquire about the various courses either by phone or by email of the course coordinator:
Course Coordinator: Ishant Kumar Bajpai, Scientist 'D'
Email: ishant@nielit.gov.in
Mobile(WhatsApp): 09445240125

Placement:

Students, who have completed the course successfully and are qualified, will be given placement guidance and career counseling to crack the interviews.

Important Dates

Last Date of Registration: 18-02-2024

Date of publishing Provisional Selection List: 20-02-2024

Course Start Date: 22-02-2024

Examination & Certification

- ✓ Final Certificates will be issued after the successful completion of all the modules. For getting a certificate a candidate has to pass each module individually with minimum required mark of 50%.

Examination Scheme

The examination scheme for each module is as follows:

Module Name	Total Marks	Written	Practical / Assignment
VLSI Fundamentals	50	10	40
CMOS Transistor Theory	**50**	10	40
Designing RTL circuits using Verilog hardware description language	**75**	20	55
FPGA based system design and emulation	**125**	25	100
Total	**300**	**65**	**235**

Grading Scheme

- ✓ Following Grading Scheme (on the basis of total marks) will be followed:

Grade	**S**	**A**	**B**	**C**	**D**	**Fail**
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

- ✓ Final Grading as per the above grading scheme will be given on the basis of total marks obtained in all modules.

Lab Infrastructure Details:

Hardware Facilities:

- ✓ FPGA-Zed Board,
- ✓ Kintex, Virtex, Zynq,
- ✓ DE0 Development,
- ✓ Anvyl & Atlys Spartan-6,
- ✓ Zybo Board

Software Facilities:

- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ Matlab

Faculty Profile

Ishant Kumar Bajpai

Scientist 'D'

Ishant Kumar Bajpai, Scientist 'D', NIELIT Chennai Has more than 10 years of experience in the Coordination and Implementation of funded projects in the area of IoT and VLSI with the application in Biomedical & Automotive. He has successfully executed 1 funded capacity-building project in Karnataka & Kerala State and was involved in the implementation of 4 skill development /capacity-building projects funded by MeitY in the states of Tamil Nadu, Andhra Pradesh, and Telangana. Before joining NIELIT, he was working as a Scientific Officer in the IT Research Academy Division of Digital India Corporation (erst. Media Lab Asia), where he was involved in the Project Planning, Design, and Implementation of projects in the domain of Mobile Computing, Networking & Applications.

Chandralakha R Pillai

Resource Person- (Embedded & VLSI)

Chandralakha R Pillai, Resource Person- Embedded and VLSI having 3 years of experience in edtech industry as well as hands on experience on PCB design in altium designer with the background of M Tech in VLSI and embedded systems.

Annexure

Detailed Syllabus of the Course

VL 311: VLSI fundementals

Duration: 10 Hours

Course Description

- Overview of VLSI technology and its significance
- Introduction to VLSI design flow: Front-end and Back-end

VL312: CMOS Transistor Theory

Duration: 10 Hours

Course Description

- Fundamentals of MOSFET operation .
- CMOS Inverter Characteristics
- CMOS Logic Design
- Transistor Level Schematics and Layouts
- On-Chip Wire Modeling
- Bonding Diagram, Packaging, and Assembly
- Combinational Logic Circuit Critical Path Optimization
- Timing in Sequential Circuits

VL313: Designing RTL circuits using Verilog hardware description language

Duration: 10 Hours

Course Description

- Introduction to Verilog HDL-Module, Ports and Data Type

- Gate Level, Data Flow, and Behavioural Modeling
- Logical, Conditional, and Lopping statements

- IP Intergrator based system development
- RTL Design Methodology
- RTL Design Using HDL.
- RTL Simulation and Verification.
- Timing Constraints and Analysis.

VL314: FPGA-based system design and emulation

Duration: **10** Hours

Course Description

- Introduction to FPGAs
- FPGA Architecture and Components.
- FPGA Design Flow.
- FPGA Design Optimization Techniques.
- ARM based processor design on the FPGA
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