COURSE PROSPECTUS

Name of the Group: *VLSI Design Group*
Name of the Course: *Advanced Diploma in VLSI Design & Verification*
Course Code: *VL200*
Starting Date: *15.05.2019*
Duration: *04 Months*
Course Coordinator: *Nandakumar.R, +91 9995427802*

Preamble: VLSI Design flow for bringing up digital Application Specific Integrated Circuits (ASICs) comprises three basic phases viz Design, Verification and Test. The VL200 course is conceived to impart the participants with comprehensive idea of the challenging tasks of Design and Verification of digital Intellectual property cores for VLSI
The course covers state of the art, cutting edge CAD tools and methodologies used in standard industry practices

Objective of the Course: The *Advanced Diploma in VLSI Design & Verification* is intended to impart training in designing and verifying reusable Intellectual Property (IP) Cores for VLSI. Emphasis of the teaching curriculum is on design & Verification methodologies and on its practical applications. The course contents have been designed keeping in view the emerging trends in needs for skilled manpower. The course is highly practical oriented with 75 % of time spend on hands on practices by the candidates

The curriculum has been designed in consultation with industry and academic experts and our strategic partners, to map the skill sets and design methodologies, which is high in demand in VLSI & Embedded Systems industries. Our students have been successfully placed in reputed product companies and we enjoy the trust of many reputed companies, who have entered into strategic alliances with us.

Outcome of the Course:

VL200 course is uniquely designed to produce the following outcome;

To produce trained candidates having highest caliber with the following attributes;

1. Sharp practical and experimentation skills
2. Thorough working knowledge in EDA tools used in the industry
3. Proficiency in industry standards and methodologies for design and verification for VLSI
4. Capability for self learning and quick adaption to agile environments
5. Ability to independely handle VLSI deign and verification responsibilities

Course Structure: The VL200 program contains five modules. The students are required to do a project work in any one of the modular areas, for a period of 6 weeks to be eligible for issue of the advanced diploma

The modules are as follows:

Module No	Module Name	Duration (Weeks)
Module 1	Foundation	1
Module 2	Verilog HDL : Language and Coding for Synthesis	2
Module 3	FPGA Based prototyping	1
Module 4	RTL Verification (System Verilog, UVM)	6
Module 5	Project Work*	6
Total		16

*With due approvals the candidates can be permitted to take up internships with core industries from start of the project phase

Other Contents

a. **Course Fees**: Rs 45,000+GST at actual (currently 18%)

General Candidates: **Rs 53,100.00** (Incl GST at current rate)

SC/ST Candidates: Tuition Fees are waived for SC/ST students admitted under SCSP/TSP.

However they are required to remit an amount of **Rs. *5,310.00*** as Advance caution/security deposit. This amount will be considered as caution/security deposit and **will be refunded** after successful completion of the course.

If the student fails to complete the course successfully this amount along with any other caution/security deposits by the student will be forfeited.
Modular wise Course Fee: Not Applicable for this course

b. **Registration Fee:** An amount of Rs.1000/- (including GST) (nonrefundable) should be paid at the time of registering for the course. (Registration fee not applicable for SC/ST Students)

However above the registration fee shall be refunded on few special cases as given below

- Student register and pay fee for more than one course and join for any one course, fee paid for remaining shall be refunded
- Course postponed and new date is not convenient for the student
- Course cancelled in advance, well before the admission date

c. **Course Fee Installment Structure**:
Students can pay the full fees of *53100.00 (*Rs. *45,000 + GST@ 18%*) in advance or as installments as given below

Fees	*Amount for General Candidates	Amount for SC/ST Candidates	Due Date (on or before)
First Installment	*Rs 30,000.00*	Rs.*8260.00* (refundable after successful completion of course)	*8.05.2019*
Last Installment	*Rs 23100.00*	Not applicable	*15.05.2019*

* Fees is inclusive *GST* @actual (*18%*) and revision if any will be applicable at the time of payment.

Fine will be applicable to late fee payment as given below

Sl. No.	Description	Fine
1	Late fee payment within two weeks after due date	18% (annually) of the outstanding dues
2	After second week of due date the candidate has to pay readmission fees along with the fine	Readmission fee Rs. 250/- plus fine of 18% (annually) of the outstanding dues
3	The candidate has to discontinue the course after third week from the due date	

d. **Eligibility:**
M.E/M.Tech/B.E/B.Tech(ECE/EEE/AEI/CSE/IT/Biomedical/Medical Electronics, Mechatronics and allied branches) OR M.Sc (Electronics/CS). Graduates with appropriate experience and final year students also may apply.

Final year students have to include the copies of course completion certificate of their qualifying degree/ diploma or copies of the mark lists up to the last semester/ year. On the date of counseling/ admission, he/she must produce the originals of course completion certificate/ mark lists up to the last semester/year examination.

For more details about the policy refer:
http://nielit.gov.in/sites/default/files/course/NIELITCalicutPoliciesShortTermCourses.pdf

e. **Number of Seats :** *25*

f. **How to Apply :**
Students are advised to apply online @ ***http://nielit.gov.in/content/online-registration.*** Payment towards nonrefundable registration fee of Rs.1,000/- (not applicable for SC/ST students) *may be paid through online payment gateway available in the Registration page or through any of the mode of payments specified in* ***http://nielit.gov.in/calicut/content/mode-payments-0***

The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

g. **Selection of candidates:** Selection is based on the marks in the qualifying Degree

h. **Test/Interview (*if applicable*) :** *Not Applicable*

i. **Counseling/Admission** : *15.05.2019*

j. **Spot Admission:** Unfilled/vacant seats are filled through spot admission. Spot admission (if open) will close within 15 days of Counseling/Admission of a particular course. On spot admission students should provide an undertaking saying that he/she is fully aware that he/she missed so much days of class and will not ask for extra classes or further extension of course.

k. **Admission Procedure :**

Students who have been selected for test/interview/counseling/admission are required to report to the Institute on the prescribed day by 9:30 hrs along with the following

- **Original and self attested Copies of Proof of Age, Qualifications, etc.**
- **One passport size photograph for identity card.**
- **SC/ST Certificate (Original and two attested copies, if applicable).**
- **Govt. issued photo ID card (Aadhaar mandatory for SC/ST candidates. Original and one copy)**

l. **Discontinuing the course:** No fees (including the caution/security deposit) under any circumstances, shall be refunded in the event of a student discontinuing the course. No certificate shall be issued for the classes attended.

A student can however, be eligible for module certificates (applicable only for courses which provide for modular admission) which he has successfully completed provided, he/she has paid the entire course fees. This is not applicable to SC/ST candidates availing fee concession. SC/ST candidates availing fee concession are eligible for module certificates only after completing the full course with required attendance

m. **Course Timings** : *9.30 am to 4.45 pm*

n. **Location and how to reach :**

NIELIT Calicut is located very close to NIT campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses (Buses to NIT via Kunnamangalam) are available from "Palayam Bus Stand and KSRTC Bus Stand". The bus stop at our Institute is called "Panthrand" and is one stop before NIT. The bus fare is around Rs.20/- from Calicut City to NIELIT.

Calicut (Kozhikode) is well connected by Rail, Road and Air form different parts of the country. The maximum and minimum temperatures range between 35^{o}C and 20^{o}C.

o. **Course enquiries :**

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

p. **Important Dates (if applicable) :**

Last date for receiving completed application forms	01.05.2019
Publication of selection list in the institute's Website	02.05.2019 (after 4.00 pm)
Last date for payment of first installment of fee	8.05.2019
Counseling/commencement date	15.05.2019
Payment of last installment fees	15.05.2019

q. **Placement** : *visit http://nielit.gov.in/content/placement-3*

r. Hostel facilities :

Hostel accommodation is available for boys and girls on monthly or daily chargeable basis. The hostel fee varies from Rs.1,400 /- to Rs.1,500/- per month depending on the type of accommodation. However, students are required to pay the hostel fees for the entire duration of the course for which they are seeking admission at the time of joining the course itself.

s. Boarding facilities :

Canteen & Mess facility is available for both boys & girls, students, those who avail mess facility should pay monthly mess fee @Rs.130/*- per day. An amount of Rs.1,000/- should be paid as mess advance to the Canteen Contractor at the time of joining the mess which will be adjusted in the last month mess fee.

as per the present rate of contract agreement

An amount of Rs.3,000/- should be paid as caution deposit (hostel & mess) at the time of joining the hostel which will be refunded/adjusted at the end of the course. For students not availing hostel facility, Rs.1,000/- will be the caution deposit

t. **Lab Facilities** : *http://nielit.gov.in/calicut/calicut/content/vlsi-design-group*

u. **Course Contents :**

Module 1: Foundation (1 Week)

- Refresher on Digital System Design fundamentals
- Introduction to Linux
- Introduction to Scripting
- IC Fabrication Flow

Module 2: Verilog HDL: Language and Coding for Synthesis (2 week)

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Gate Level Modeling, Dataflow Modeling, Behavioral Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Mini project and Case Studies

Module 3: FPGA Design Methodology and Prototyping (1 week)

- Introduction to Programmable Logic and FPGAs
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow Xilinx Vivado
- Implementation Procedure
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Design problems using Xilinx Platforms

Module 4: RTL Verification (System Verilog, UVM) (6 week)

- Functional Verification –Concepts, Simulators, Coverage and Metrics,
- Introduction to Verification Methodologies, Testing strategy Directed and random Testing, Test Cases Vs Test Benches, Verification Components (Drivers, Checkers, Monitors, Scoreboardsetc),
- System Verilog, Object oriented programming for ASIC Verification
- Functional Verification, Assertion based verification, Coverage Driven
- Verification, Coverage Analysis, PLI and DPI Basics, Universal Verification Methodology, UVM Components and practices, Case Study- Verification IP Design

Module 5: Projects (6 week)

The candidates are required to complete a project work on VLSI Design and/or Verification, for a period of 6 weeks to be eligible for issue of diploma.